In the Claims

Please replace all prior versions, and listings, of claims in the application with the following list of claims:

1. (Currently amended) A scanning circuit, comprising:

a power supply providing a negative voltage on a first terminal, an intermediate voltage on a second terminal and a positive voltage on a terminal of a switch, the other terminal of the switch being connected to a third terminal,

a control circuit supplied by connections to the second and third terminals,

a differential amplifier receiving a positive and a negative input signal provided by the control circuit,

a power amplifier controlled by the differential amplifier, both amplifiers being supplied by connections to the first and third terminals,

a deflection coil connected between the output of the power amplifier and the second terminal,

biasing means for setting, when the switch is open, the output of the differential amplifier so that ~~the possible~~ a current path [[paths]] through the power amplifier between the deflection coil and the first terminal ~~are cut~~ is substantially eliminated.

2. (Previously Presented) A scanning circuit according to claim 1, wherein the differential amplifier comprises eight transistors, the third and fourth transistors being of NPN type, the other transistors of PNP type, the base of the first transistor receiving the negative input signal, the base of the second transistor receiving the positive input signal, the emitters of the first and second transistors being connected to the collector of the sixth transistor, the emitter of the sixth transistor being connected to the third terminal, the base of the sixth transistor being connected to the collector of the eighth transistor, the base of the eighth transistor being connected to its collector, the emitter of the eighth transistor being connected to the third terminal, the collector of the eighth transistor being connected to a current source, the collector of the first transistor being linked to the first terminal by a first resistor, the collector of the

second transistor being linked to the first terminal by a second resistor, the bases of the fifth and seventh transistors being connected to the base of the sixth transistor, the emitters of the fifth and seventh transistors being connected to the third terminal, the collector of the fifth transistor being connected to the collector of the third transistor, the emitter of the third transistor being connected to the collector of the first transistor, the collector of the third transistor being connected to its base, the collector of the seventh transistor being connected to the collector of the fourth transistor, the emitter of the fourth transistor being connected to the collector of the second transistor, the base of the fourth transistor being connected to the base of the third transistor.

3. (Previously Presented) A scanning circuit according to claim 2, wherein a comparator receives on a first input a fixed voltage equal to the voltage of third terminal minus the voltage of a reference supply, the other input of the comparator being connected to the collector of the sixth transistor, a reference current source controlled by the comparator being connected to the collector of the third transistor.

4. (Currently amended) A scanning circuit according to claim 2, wherein an auxiliary P-type zone is provided near [[the]] a P-type zone forming the collector of the sixth transistor, the auxiliary P-type zone being connected to the collector of the third transistor.

5. (Previously Presented) A scanning circuit according to claim 2, wherein a P-type zone forms the common emitters of the fifth, sixth and seventh transistors, a N-type zone surrounding the emitter forms the common base of the transistors, three P-type zones surrounding the common base form the collectors of the transistors, all collectors being separated by narrow N-type zones, the length of opposite outlines of the collectors of the fifth and sixth transistors being larger than the length of opposite outlines of the collectors of the seventh and sixth transistors.

6. (Previously Presented) A scanning circuit according to claim 1, wherein the differential amplifier comprises an input transistor pair receiving the positive and the negative input signals, the input transistor pair forming a first amplifying stage coupled to a second

amplifying stage, and wherein the sizes of the transistors of the input transistor pair are different and wherein the sizes of the components of the second amplifying stage are different to balance the transistor size difference of the input transistor pair when the switch is open.

7. (New) A scanning circuit, comprising:

a switch;

a first supply terminal coupled to the switch;

a deflection coil;

a power amplifier coupled to the first supply terminal and the deflection coil;

a differential amplifier having an output coupled to the power amplifier; and

at least one biasing component that sets an output of the differential amplifier to a determined voltage such that a current path through the power amplifier is substantially eliminated, the output of the differential amplifier being set to the determined voltage in response to a voltage of the first supply terminal reaching a threshold.

8. (New) The scanning circuit of claim 7, wherein the at least one biasing component comprises a comparator.

9. (New) The scanning circuit of claim 8, wherein the at least one biasing component further comprises a reference voltage source having a first terminal coupled to a first input of the comparator and a second terminal coupled to the first supply terminal.

10. (New) The scanning circuit of claim 9, wherein the at least one biasing component further comprises a first transistor having an emitter coupled to the first supply terminal and a collector coupled to a second input of the comparator.

11. (New) The scanning circuit of claim 8, further comprising a current source coupled to an output of the comparator.

12. (New) The scanning circuit of claim 11, wherein the current source is further coupled to the voltage supply terminal and a second transistor.

13. (New) The scanning circuit of claim 12, wherein the current source is coupled to a collector and base of the second transistor.

14. (New) The scanning circuit of claim 12, wherein the current source provides a current to the second transistor in response to the voltage of the first supply terminal reaching the threshold.

15. (New) The scanning circuit of claim 7, wherein the determined voltage is a low voltage.

16. (New) The scanning circuit of claim 7, wherein the at least one biasing component comprises transistors coupled to the first supply terminal having different sizes such that the output of the differential amplifier is set to the determined voltage in response to a voltage of the first supply terminal reaching the threshold.

17. (New) The scanning circuit of claim 16, wherein at least two of the transistors have collectors of different sizes, a common base, and a common emitter coupled to the first supply terminal.

18. (New) The scanning circuit of claim 7, wherein the at least one biasing component comprises a first transistor having an emitter coupled to the first supply terminal and an auxiliary collector coupled to the base and collector of a second transistor.

19. (New) The scanning circuit of claim 7, wherein the threshold is approximately zero volts.

20. (New) The scanning circuit of claim 7, wherein the voltage of the first supply terminal reaches the threshold in response to a transition of the switch from an on state on an off state.